CLAIMS

Therefore, having thus described the invention, at least the following is claimed:

1. A method for fabricating micro-electro-mechanical system (MEMS) capacitive resonators, the method comprising:

forming trenches in a substrate;

conformally coating the substrate with an oxide;

filling the coated trenches with polysilicon;

patterning the polysilicon;

releasing a resonator structure derived from the substrate; and

removing the conformally coated oxide.

2. The method of claim 1, further comprising:

depositing nitride on at least one of an insulating layer and the substrate;

patterning the nitride to isolate pads;

providing polysilicon to the patterned pads; and

metallizing the pads.

3. The method of claim 1, wherein the releasing comprises separating the resonating structure from the polysilicon.

4. The method of claim 1, wherein the releasing comprises an isotropic silicon etching of the resonator.

5. The method of claim 1, wherein the filling includes filling out from sidewalls of the trenches.

6. The method of claim 1, wherein the removing includes forming a gap between the resonator structure and the polysilicon in a self-aligned manner.

7. The method of claim 6, wherein the gap is approximately less than 90 nanometers.

8. The method of claim 1, wherein the filling includes forming an electrode.

9. The method of claim 1, wherein the etching includes forming high-aspect ratio trenches.

10. A micro-electro-mechanical system (MEMS) capacitive resonator, comprising:

a semiconductor resonating member; and

a polysilicon electrode comprised of a different material than the semiconductor resonating member, wherein the polysilicon electrode is capacitively coupled to the semiconductor resonating member.

11. The resonator of claim 10, wherein the polysilicon electrode is capacitively coupled to the semiconductor resonating member over a gap ranging from one of approximately 700 – 1000 nanometers (nm), 90 – 700 nm, and less than 90 nm.

12. The resonator of claim 10, wherein the semiconductor resonating member has a width ranging from approximately 5.5 – 7.5 microns, a length for the corresponding width ranging from approximately 300 – 1100 microns, a first flexural mode frequency response for the corresponding width and length ranging from approximately 40 kilohertz – 528 kilohertz, and a quality factor for the first flexural frequency response ranging from approximately 17,000 – 67,000.

13. The resonator of claim 10, wherein the semiconductor resonating member has a width of approximately 5.5 – 6.5 microns, a length for the corresponding width ranging from approximately 300 – 1100 microns, a first flexural mode frequency response for the corresponding width and length ranging from approximately 40 kilohertz – 528 kilohertz, and a quality factor for the first flexural frequency response ranging from approximately 17,000 – 67,000.

14. The resonator of claim 10, wherein the semiconductor resonating member includes one of a beam and a block.

15. The resonator of claim 10, wherein the semiconductor resonating member has a thickness ranging from one of 5 microns to 40 microns, 10 to 40 microns, 20 to 40 microns and 30-40 microns.

16. The resonator of claim 10, wherein the resonator is a MEMS device.

17. The resonator of claim 10, wherein a gap inherent to the capacitive coupling is formed in a self-aligned manner using a sacrificial layer in between the semiconductor resonating member and the polysilicon electrode.

18. A method for fabricating micro-electro-mechanical system (MEMS) capacitive resonators, the method comprising:

forming trenches in a semiconductor-on-insulator substrate;

conformally coating the semiconductor-on-insulator substrate with an oxide;

filling the coated trenches with polysilicon, wherein electrodes are derived from the polysilicon;

forming release openings; and

removing the conformally coated oxide and an oxide of the semiconductor-on-insulator substrate, wherein a capacitive gap is formed, wherein a resonating element of the capacitive resonator is released.

19. The method of claim 18, further including:

growing and patterning an insulator oxide, wherein the insulator oxide provides isolation between the semiconductor-on-insulator substrate and wire-bonding pads;

depositing and patterning nitride, wherein the nitride provides protection for the insulator oxide disposed on the pads;

growing and removing a surface treatment oxide, wherein the surface treatment oxide enables the reduction of the roughness of sidewalls of the resonating element;

depositing polysilicon to form the wirebonding pads for drive and sense electrodes;

metallizing the pads; and

patterning the polysilicon inside the trenches.

20. The method of claim 18, wherein the forming release openings comprises anisotropically etching to an oxide layer of the semiconductor-on-substrate, such that the undercut of the resonating element is facilitated.

21. The method of claim 18, wherein the filling includes one of filling the trenches with doped LPCVD polysilicon such that the electrodes are formed vertically and depositing and patterning doped LPCVD polysilicon.

22. The method of claim 18, wherein the forming trenches includes one of deep reactive ion etching and regular reactive ion etching to an oxide layer of the semiconductor-on-insulator substrate.

23. The method of claim 18, wherein the conformally coating includes depositing a LPCVD high-temperature oxide of approximately less than 100 nanometers.

24. The method of claim 18, wherein the conformally coating is scalable to correspond to a desired thickness of a lateral gap spacing for the capacitive resonator.

25. The method of claim 18, wherein the removing comprises an anisotropic plasma etching such that at least a portion of the oxide remains on sidewalls of the resonating element.

26. The method of claim 18, wherein the releasing comprises exposing the semiconductor-on-insulator substrate to a solution comprising HF:H20 to release the resonating element from a handle layer and the electrodes.

27. The method of claim 18, wherein the forming trenches includes etching high-aspect ratio trenches.

28. The method of claim 18, wherein the removing includes forming a gap between the resonating element and the polysilicon in a self-aligned manner.

29. A semiconductor-on-insulator (SOI) micro-electro-mechanical system (MEMS) capacitive resonator, comprising:

a semiconductor resonating member; and

a polysilicon electrode comprised of a different material than the semiconductor resonating member, wherein the polysilicon electrode is capacitively coupled to the semiconductor resonating member.

30. The resonator of claim 29, wherein the polysilicon electrode is capacitively coupled to the semiconductor resonating member over a gap of approximately 90 nanometers.

31. The resonator of claim 29, wherein the semiconductor resonating member has at least one of a flexural and bulk-mode frequency response ranging from approximately 3 MHz – 300 MHz and a quality factor over at least one of approximately 10,000, 20,000, and 30,000.

32. The resonator of claim 29, wherein the semiconductor resonating member includes one of a disk, a beam, and a block.

33. The resonator of claim 32, wherein the disk is supported on its side at one of a location corresponding to a resonating node and a plurality of resonating nodes.

34. The resonator of claim 29, wherein the semiconductor resonating member has a thickness ranging from one of 5 microns to 40 microns, 10 to 40 microns, 20 to 40 microns and 30-40 microns.

35. The resonator of claim 29, wherein a gap inherent to the capacitive coupling is formed in a self-aligned manner using a sacrificial layer in between the semiconductor resonating member and the polysilicon electrode.